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10/624,801	07/22/2003	Yoji Idei	KAM-00801	7476

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EXAMINER	
NGUYEN, HAI L	

ART UNIT	PAPER NUMBER
2816	

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Patent Group
Choate, Hall & Stewart
Exchange Place
53 State Street
Boston, MA 02109-2804

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/624,801	IDEI, YOJI	
	Examiner	Art Unit	
	Hai L. Nguyen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 April 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *19 April 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *7/20/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the details of operating of the first and second bi-directional delay circuit strings, such as "each circuit string having an input terminal and an output terminal, in which an edge of a clock signal received at the input terminal proceeds in one direction and then is reversed in the proceeding direction thereof, based on a turn control signal generated on the basis of an edge of a clock signal next following the input clock signal, the clock edge proceeding in the direction reverse to the one direction, over a time equal to the time during which the clock edge proceeded in the one direction, so as to be output at the output terminal" in claim 1; and "means for comparing", in claim 14, must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted

by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

2. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Objections

3. Claim 6 is objected to because of the following informalities: lines 2-3, "the delay time of" should be deleted. Appropriate correction is required.

4. Claim 16 is objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form. A semiconductor device limitation of claim 16 does not further define the clock synchronization circuit of claim 1.

Claim Rejections - 35 USC § 112

5. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

6. Claims 1-20 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in

the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. The claimed limitation that "first and second bidirectional delay circuit strings, ..., in which an edge of a clock signal received at the input terminal proceeds in one direction and then is reversed in the proceeding direction thereof, based on a turn control signal generated on the basis of an edge of a clock signal next following the input clock signal, the clock edge proceeding in the direction reverse to the one direction, over a time equal to the time during which the clock edge proceeded in the one direction, so as to be output at the output terminal", in claim 1, has not been enabled in the specification. The details of such functions are not seen in the description of the preferred embodiment. It is not clear as currently defined, how the instant invention can perform the recited function. Furthermore, claim 17 has a similar problem.

7. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

8. Claims 17-20 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 17 recites the limitation "said second buffer" in lines 31-32. There is insufficient antecedent basis for this limitation in the claim. Furthermore, the recited limitation "a second control circuit (105 in instant Fig.1) receiving an output signal of said second buffer", lines 31-32, is misdescriptive. Fig. 1 clearly shows that there is only one single buffer circuit (101), which already recited in lines 24-25 as a first buffer circuit, i.e., a first control circuit (104 in instant Fig.1) receiving an output signal of said first buffer circuit".

Claims 18-20 are rendered indefinite by the deficiencies of base claim 17.

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. Claims 1-7, 10, 13, 15, 17, and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over the admitted prior art, Fig. 9A in the present application, in view of Isobe et al. (US 6,359,480) and further in view of Farwell (US 5,870,445).

With respect to claim 1, the admitted prior art in Fig. 9A shows a clock synchronization circuit comprising first and second bi-directional delay circuit strings (406, 407); a multiplexing circuit (408); and phase selection controlling means (403). Fig. 9AB of the prior art meets all the claimed limitations, except for a pre-stage delay circuit and a post-stage delay circuit, arranged at a pre-stage and at a post-stage of the bi-directional delay circuit string, respectively. Isobe et al. teaches in Fig.1 a circuit having a pre-stage delay circuit (12, 13) and a post-stage delay circuit (17), arranged at a pre-stage and at a post-stage of the delay circuit string (14-16, a.k.a. bi-directional delay circuit strings) as recited in the claim. Since Fig. 1 of Isobe et al. and the admitted prior art (Fig. 9A) are similar because they are clock synchronization circuits, it would have been obvious to one of ordinary skill in the art at the time of applicant's invention was made to utilize a pre-stage delay circuit and a post-stage delay circuit taught by Isobe et al., arranged at a pre-stage and at a post-stage of the bi-directional delay circuit strings (406 & 407 in

instant Fig. 9A in the present application) of the admitted prior art, respectively, in order to causes the internal clock signal to be synchronized with the external clock signal in such a manner that the former is shifted half the period from the latter. However, the pre-stage delay circuit and a post-stage delay circuit taught by Isobe et al. are not being able to be variably set as recited in the claim. Farwell et al. teaches in Fig. 3 a delay circuit ($I_{(1)}$-$I_{(N)}$, $M_{(1)}$-$M_{(N)}$) having delay times that can be variably set by a delay time setting circuit (51). Therefore, it would have been obvious to one of ordinary skill in the art at the time of applicant's invention was made to replace the pre-stage and post-stage delay circuits of the references (Isobe et al.) with variable delay circuits and delay time setting circuits for the advantage being able to change delay time of the pre-stage and post-stage delay circuits at a desirable delay time by using the control signal without replacement of the existing delay circuits.

With regard to claims 2-4, 10, and 15, the references (Fig. 9A of the admitted prior art) also meet the recited limitations in these claims.

With regard to claims 5 and 13, the references also meet the recited limitations in these claims. Since the claimed structure is met by the references, inherently, the result functions of these claims will also be met.

With regard to claim 6, each of the pre-stage and post-stage delay circuits includes a plurality of stages of delay elements ($I_{(1)}$-$I_{(N)}$, $M_{(1)}$-$M_{(N)}$); and a plurality of stages of selection circuits ($S_{(1)}$-$S_{(N)}$) selecting delay elements among the plurality of stages of the delay elements that make up a delay line, wherein a delay time corresponding to a tap selection signal (CONTROL) selected among a plurality of tap selection signals supplied from the delay time setting circuit is set.

With regard to claim 7, each of the pre-stage and post-stage delay circuits includes a signal input terminal (input terminal of I(1)); a signal output terminal (output terminal of M(1)); a plurality of control signal input terminals for receiving a plurality of tap selection signals (Ss) supplied from the delay time setting circuit (51); a first stage selection circuit selecting one of the clock signal supplied from the signal input terminal and a signal of a fixed logic value in accordance with a value of the corresponding first tap selection signal; and a plurality of unit delay circuits connected in cascade connection and arranged downstream of the first stage selection circuit; each unit delay circuit including: a delay element receiving an output of a selection circuit of the preceding stage; and a selection circuit selecting one of the clock signal supplied from the signal input terminal and the output of the delay element, based on the value of the corresponding tap selection signal; and wherein the clock signal supplied from the signal input terminal is propagated from the selection circuit of the unit delay circuit corresponding to the selected tap selection signal to the delay element of the unit delay circuit of the next stage and output from the signal output terminal through the unit delay circuit inserted between the unit delay circuit of the next stage and the signal output terminal.

Claim 17 is similarly rejected; note the above discussion with regard to claims 1-3.

Claim 18 is similarly rejected; note the above discussion with regard to claim 7.

Conclusion

11. Regarding claims 8, 9, 11, 12, 14, 16, 19, and 20, the patentability thereof cannot be determined because of failing to comply with the enablement requirement.

12. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. For example, Okuda et al. (US 6,437,619) is cited as of interest because it discloses a clock generation circuit, control method of clock generation circuit, clock reproducing circuit, semiconductor memory device, and dynamic random access memory.

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hai L. Nguyen whose telephone number is 571-272-1747 and Right Fax number is 571-273-1747. The examiner can normally be reached on Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 571-272-1740. The official fax phone number for the organization where this application or proceeding is 703-872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 571-272-1562.

HLN
June 18, 2004

TIMOTHY P. CALLAHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800